REMARKS/ARGUMENTS

Claims 15, 27, 35-39 and 41 are pending in the present application, of which Claims 15, 27 and 37 are the independent claims. No new claims have been added. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 103

Claim 15 is rejected under 35 USC § 103(a), as being unpatentable over U.S. Patent Application Publication No. 2003/0127747 ("Kajiwara") in view of U.S. Patent Application Publication No. 2003/0146518 ("Hikita"). Reconsideration and withdrawal of the rejection are respectfully requested.

Independent Claim 15 is generally directed to a method associated with a semiconductor wafer. The method includes (i) providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes (ii) providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump used for a package interconnect wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. The method also includes (iii) performing a sputter etching process with an argon gas after providing the exposed metallization structure and prior to wafer testing the semiconductor wafer. As indicated above, Claim 15 has been amended to specify that the sputter etching process with an argon gas is performed prior to wafer testing the semiconductor wafer. Support for this amendment may be found at least on page 6 of the originally filed application. These features are not seen to be disclosed or suggested by Kajiwara and Hikita individually or in combination.

With respect to the applied reference, Kajiwara is directed to a semiconductor device in which an LSI chip comprising electrodes with a 100μm pitch or less and 50 or more pins is

mounted directly to the organic substrate. See Kajiwara, Abstract and paragraph 17. Electrode Au bumps of the chip and an Au film at the uppermost surface of connection terminals of the substrate are directly flip-chip bonded by Au/Au metal bonding. See Kajiwara, Abstract and paragraph 17. The method of obtaining the bonded structure involves a process of supersonically bonding both of the bonding surfaces within 10 minutes after sputter cleaning. See Kajiwara, Abstract and paragraph 17.

The Office Action contends that sputter etching of the Au bump surface mentioned in paragraph 39 of Kajiwara corresponds with the sputter etching process recited in Claim 15. Applicants respectfully disagree. As noted above, Claim 15 has been amended to specify that the sputter etching process is performed prior to wafer testing the semiconductor wafer. Kajiwara, on the other hand, performs the referenced sputter etching of the Au bump in the flip-chip bonding step. At the flip-chip bonding step, the semiconductor wafer from which the chip, such as semiconductor chip 6, was diced already would have undergone any wafer testing. Accordingly, the sputter etching process referenced in Kajiwara would follow rather than proceed any wafer testing.

Hikita, which was applied in combination with Kajiwara as allegedly teaching a method for fabricating a circuit component wherein a metal bump having the features recited in Claim 15, is not seen to disclose or suggest anything the remedy the foregoing deficiencies of Kajiwara discussed above. Therefore, independent Claim 15 is believed to be allowable over Kajiwara and Hikita. Reconsideration and withdrawal of the § 103(a) rejection of Claim 15 are respectfully requested.

Claim 35 is rejected under 35 USC § 103(a), as being unpatentable over Kajiwara in view of Hikita, as applied to claim 15, and further in view of U.S. Patent No. 6,162,652 ("Dass"). Reconsideration and withdrawal of the rejections are respectfully requested.

Claim 35 in the application is dependent from independent Claim 15. Dass is not seen to remedy the deficiencies of Kajiwara and Hikita discussed above. Accordingly, Claim 35 is believed to be allowable over the applied references for at least the same reasons as discussed above with respect to Claim 15. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merit is respectfully requested.

Claims 27, 37 and 38 are rejected under 35 USC § 103(a), as being unpatentable over Kajiwara in view of U.S. Patent No. 6,956,292 ("Fan") and Hikita. Reconsideration and withdrawal of the rejection are respectfully requested.

Independent Claim 27 is generally directed to a method associated with a semiconductor wafer. The method includes (i) providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes (ii) providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump used for a package interconnect wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. The method also includes (iii) performing an ion milling process with an argon gas after providing the exposed metallization structure and prior to wafer testing the semiconductor wafer. As indicated above, Claim 27 has been amended to specify that the sputter etching process with an argon gas is performed prior to wafer testing the semiconductor wafer. Support for this amendment may be found at least on page 7 of the originally filed application. These features are not seen to be disclosed or suggested by Kajiwara, Hikita and Fan individually or in combination.

As discussed above with respect to independent Claim 15, Kajiwara and Hikita are not seen to disclose or suggest the step of performing a sputter etching process with an argon gas prior to wafer testing. It follows that Kajiwara, Hikita and Fan, which was applied in combination with Kajiwara and Hikita for its disclosure of an ion milling process using argon gas, are also not seen to disclose or suggest at least the step of performing an ion milling process with an argon gas prior to wafer testing.

Independent Claim 37 is generally directed to a method associated with a semiconductor wafer. The method includes (i) providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said

second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes (ii) providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump used for a package interconnect wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. The method also includes (iii) performing an ion milling process with an inert gas after providing the exposed metallization structure and prior to wafer testing the semiconductor wafer. As indicated above, Claim 37 has been amended to specify that the sputter etching process with an inert gas is performed prior to wafer testing the semiconductor wafer. Support for this amendment may be found at least on page 7 of the originally filed application. These features are not seen to be disclosed or suggested by Kajiwara, Hikita and Fan individually or in combination.

As discussed above with respect to independent Claim 15, Kajiwara and Hikita are not seen to disclose or suggest the step of performing a sputter etching process with an argon gas prior to wafer testing. It follows that Kajiwara, Hikita and Fan, which was applied in combination with Kajiwara and Hikita for its disclosure of an ion milling process using an inert gas, are also not seen to disclose or suggest at least the step of performing an ion milling process with an inert gas prior to wafer testing.

Therefore, independent Claims 27 and 37 are believed to be allowable over the applied references. Reconsideration and withdrawal of the § 103(a) rejection of Claims 27 and 37 are respectfully requested.

Claim 38 depends from independent Claim 37 and therefore is believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

Claims 36 and 41 are rejected under 35 USC § 103(a), as being unpatentable over Kajiwara in view Fan and Hikita, as applied to claims 27 and 37 above, and further in view of Dass. Reconsideration and withdrawal of the rejections are respectfully requested.

Claims 36 and 41 in the application are dependent from independent Claims 27 and 37 discussed above and therefore are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merit is respectfully requested.

Claim 39 is rejected under 35 USC § 103(a), as being unpatentable over Kajiwara in view of Fan and Hikita, as applied to claim 37 above, and further in view of U.S. Patent No. 6,104,461 ("Zhang"). Reconsideration and withdrawal of the rejections are respectfully requested.

Claim 39 in the application is dependent from independent Claim 37. Zhang is not seen to remedy the deficiencies of Kajiwara and Hikita discussed above. Accordingly, Claim 39 is believed to be allowable over the applied references for at least the same reasons as discussed above with respect to Claim 37. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merit is respectfully requested.

CONCLUSION

In light of the Remarks herein, Applicants submit that the claims are now in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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